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09/008,531	01/16/1998	HOWARD E. RHODES	MIO012V2	6336

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EXAMINER
TRINH, MICHAEL MANH

ART UNIT	PAPER NUMBER
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/008,531	RHODES, HOWARD E.	
	Examiner	Art Unit	
	Michael M Trinh	2822	

-- The MAILING DATE of this communication appears on th cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-32,35,36,40-43 and 48* is/are pending in the application.

4a) Of the above claim(s) *26-30,35,36,40-43 and 48* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-25,31 and 32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

*** This office action is in response to Applicant's Amendment filed on October 24, 2002. Claims 21-32,35,36,40-43,48 are currently pending, in which claims 26-30,35-36,40-43,48 are non-elected invention.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Election/Restrictions

1. This application contains claims 26-30,35-36,40-43,48 drawn to an invention nonelected with traverse in Paper No. 26. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Claim Rejections - 35 USC § 112

2. Claims 31-32 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

As shown in Figure 4, the present application supports claim 21 for the step of "providing a substrate having at least one semiconductor layer 22; forming an underlayer 20 over the at least one semiconductor layer 22...". Claim 31 was however amended to recite "providing a substrate having at least one semiconductor layer; forming an opening in said at least one semiconductor layer, wherein said opening includes sidewalls, and forming a conductive layer over said at least one semiconductor layer...".

Thus, original specification does not support to "...form an open in said at least one semiconductor layer...and forming a conductive layer over said at least one semiconductor layer", since, as shown in Figure 4, no opening is formed in the semiconductor layer 22. Moreover, original specification support forming the conductive layer over an underlayer 20 and an insulator 23 (Fig 4), but not support forming the conductive layer over the at least one semiconductor layer, since an insulating layer (e.g. 20,23 in Figure 4) must be formed between the semiconductor layer 22 and the conductive layer 26 to provide electrical isolation.

(Dependent claim 32 is rejected as depending on rejected base claim 31)

Claim Rejections - 35 USC § 102

3. Claims 21-24,31-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Zamanian (5,793,111).

Zamanian teaches, at Figures 1-6 and cols 3-6, a method for forming a semiconductor device comprising at least the steps of: providing a substrate having at least one semiconductor layer 10 with inherent semiconductor gate electrode layers having opening including sidewalls formed thereon; forming an underlayer 28 (Fig 2) over the at least one semiconductor layer 10; forming a layer of conductive material 32/34/36 over the underlayer 28 having a topography that includes a substantially vertical component (Figs 3) and defining a localized thick region thereon; forming an overlayer 40 over said layer of conductive material; etching to form a contact hole in the overlayer 40 and in an overetch amount of the substantially vertical component (Fig 6; col 5, line 50 through col 6); and forming a contact 44 in said contact hole disposed adjacent to, in the vertical component, and contacting the vertical component (Fig 6). Re further claim 31, providing a substrate having at least one semiconductor layer; forming opening in the at least semiconductor layer 14/26 an underlayer 28 (Fig 2) over the at least one semiconductor layer 10; forming a layer of conductive material 32/34/36 over

Re claims 22 and 32, Zamanian shows the vertical component defining a localized thick region in the layer of conductive material.

Re claim 23, Zamanian shows wherein layer of conductive material having the vertical component formed as a spacer.

Re claim 24, Zamanian forms a structure 28 having an opening therein under the conductive layer and filling the opening with the conductive material to form the vertical component.

4. Claims 31-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Okada (5,399,890).

In re claim 31, Okada shows in Figures 2A-2C,3 and related text (col 6, lines 27 through col 8, line 8), a method for making a semiconductor device including the steps of: providing a semiconductor substrate having at least one semiconductor gate electrode layers formed thereon with opening having sidewalls; forming a layer of conductive material (9 in Fig 2C; or 9b/9a in Fig 3) having a topography that includes a substantially vertical component defining a localized thick region thereon; forming an overlayer 10 over said layer of conductive material (col 7, lines 1-12); and forming a contact 12 in said overlayer 10 and in the vertical component disposed adjacent to and contacting the vertical component of the layer of conductive material 9, wherein the method includes forming a structure having an opening therein and filling the opening with conductive material to form the conductive layer above the opening having the vertical component

Re claim 32, Okada shows the vertical component defining a localized thick region in the layer of conductive material.

Claim Rejections - 35 USC § 103

5. Claims 21-25,31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuo et al (5,312,769) taken with Zamanian (5,793,111) and Wolf (pages 547-554).

In re claims 21, and 31, Matsuo shows in Figures 2A-2E and related text, a process for making a semiconductor device including the steps of providing a substrate having at least one semiconductor layer 1 and with semiconductor gate electrode layers having opening including sidewalls formed thereon; forming an underlayer 21 over the at least one semiconductor layer and the opening; forming a layer of conductive material 12 over the underlayer 21 having a topography that includes a substantially vertical component defining a localized thick region; forming an overlayer over said layer of conductive material; forming contact hole in the overlayer and in an overetch amount of the substantially vertical component; and forming a contact in said contact hole disposed adjacent to and contacting the vertical component. Matsuo also shows wherein the contact hole window 29 is formed in the first interlayer insulating film 23 formed by using a dry etching technique (see Figure 2B; column 5, lines 30-46). Matsuo further shows in Figure 2B wherein the overlayer is made of oxide material and wherein the layer of conductive material is made of polysilicon (col 3, line 59 through col 5, line 55).

Matsuo fails to show etching in an overetch amount of the substantially vertical component.

However, Zamanian teaches (at Fig 6,1-5; col 5, line 50 through col 6, lines 22; cols 3-5) that in order to insure that all of the dielectric has been removed from the contact opening, etching a contact hole in the overlayer 40 and in an overetch amount of the layer of conductive material having a substantially vertical component. Wolf teaches that even though the oxide material is etched selectively to polysilicon material, some tolerable amount of polysilicon material is etched as well (pages 547-554).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the contact hole of Matsuo et al (Figure 2B) by etching a contact hole in the overlayer insulator 23 and in an overetch amount of the layer 12 of conductive material having a substantially vertical component, as combinatively taught by Zamanian and Wolf, wherein the contact is formed in the overlayer and in said vertical component. This is because of the desirability to insure that all of the dielectric of the overlayer has been completely removed from the contact hole for providing a secure and good electrical connection from the layer of conductive material to the contact.

Re claims 22 and 32, Matsuo et al shows the vertical component defining a localized thick region in the layer of conductive material.

Re claim 23, Matsuo shows wherein the vertical component is a spacer.

Re claim 24, Matsuo forms a structure 21 having an opening therein under the conductive layer 12 and filling the opening with the conductive material to form the vertical component.

Re claim 25, Matsuo shows wherein the contact 13 disposed adjacent to and contacting the vertical component 12 is a storage capacitor electrode made of the same material as the layer of conductive material (column 4, lines 3-22), in which the layer of conductive material is considered a part of the capacitor electrode.

6. Claims 21-25,31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okada et al (5,399,890) taken with Zamanian (5,793,111) and Toshiyuki et al (JP-05-109905).

In re claims 21, and 31, Okada shows in Figures 2A-2C,3 and related text (col 6, lines 27 through col 8, line 8), a method for making a semiconductor device including the steps of:

providing a substrate having at least one semiconductor layer 1; forming an underlayer 8 (Fig 2C) over the at least one semiconductor layer 1; forming over the underlayer, a layer of conductive material (9 in Fig 2C; or 9b/9a in Fig 3) having a topography that includes a substantially vertical component defining a localized thick region; forming an overlayer 10 over said layer of conductive material (col 7, lines 1-12); etching to form a contact hole 11 in the overlayer 10 and over the substantially vertical component; and forming a contact 12 in said contact hole 11 disposed adjacent to, and contacting the vertical component of the layer of conductive material 9.

Okada et al fails to show etching in an overetch amount of the substantially vertical component.

However, Zamanian teaches (at Fig 6,1-5; col 5, line 50 through col 6, lines 22; cols 3-5) that in order to insure that all of the dielectric has been removed from the contact opening, etching a contact hole in the overlayer 40 and in an overetch amount of the layer of conductive material having a substantially vertical component. Toshiyuki et al (JP-05-109905) teaches (at Figs 1-4; English abstract and Computer-English Translation pages 1-3) forming a layer of conductive material 2 over an underlayer (Fig 2); forming an overlayer 3 over said layer of conductive material (Fig 2); etching to form a contact hole 9 in the overlayer 3 and in an overetch amount of the layer of the conductive material (Fig 3,1); and forming a contact 6,8 (Figs 1,4) in said contact hole 9 disposed adjacent to, in the layer of conductive material, and contacting the layer of conductive material 2.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the contact hole of Okada et al by etching a contact hole in the overlayer insulator and in an overetch amount of the layer of conductive material having a substantially vertical component, as combinatively taught by Zamanian and Toshiyuki, wherein the contact is formed in the overlayer and in said vertical component. This is because of the desirability to insure that all of the dielectric of the overlayer has been completely removed from the contact hole for providing a secure and good electrical connection from the layer of conductive material to the contact. This is also because of the desirability to improve reliability in the multilayer interconnection structure, and to suppress occupied area of a contact part between top and bottom wiring patterns.

Re claims 22 and 32, Okada et al shows the vertical component defining a localized thick region in the layer of conductive material.

Re claim 23, Okada shows wherein the vertical component is a spacer.

Re claim 24, Okada forms a structure 8 having an opening therein under the conductive layer and filling the opening with the conductive material to form the vertical component.

Re claim 25, Okada shows wherein the conductive layer 9 is a capacitor electrode (col 6, lines 1-10).

Response to Argument

7. Applicant's remark filed October 24, 2002 have been considered but they are not persuasive and also in moot of new ground of rejections.

*** Regarding Zamanian, Applicant's remark (at 10/24/02 remark page 2) that "...claims 21 and 31 recite that the contact is formed in said contact hole...**contacting** said vertical component...Zamanian...The silicide layer 36, as shown in Fig. 5, or the barrier layer 34, as shown in Fig 6 do not allow the conductive contact 44 to contact the vertical component of conductive material 32...".

In response, it is noted and found unconvincing. In Zamanian (5,793,111), the silicide layer 36, as shown in Fig. 5, or the barrier layer 34, as shown in Fig 6 allow the conductive contact 44 to electrically contact the vertical component of conductive material 32. The comprising type method as claimed does not preclude to include an additional conductive layer therebetween.

*** Regarding rejection of claims 31-32 using Okada (5,399,890):

Applicant's remark (at 10/24/02 remark page 3, third paragraph) that "...Okada et al does not teach etching a contact hole in the overlayer and in an overetch amount of the substantially vertical component..."

In response, claims 31-32 do not recite that limitations of "...etching a contact hole in the overlayer and in an overetch amount of the substantially vertical component...". Claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. In Re Self, 213 USPQ 1,5 (CCPA 1982); In Re Priest, 199 USPQ 11,15 (CCPA 1978). As shown in the front figure,

Figures 2C,3,5,6D of Okada et al, the contact 12 formed in the vertical component of the conductive layer due to the topology or recess shape of the conductive layer 9a or 9b.

*** Regarding Matsuo in view of Zamanian and Wolf:

Applicant's remarks (at 10/24/02 remark pages 4-5) about " Wolf teaches...be etched, but not significant..." and "Zamanian teaches that significant overetch does occur..", but one ordinary skill in the art would not combine Wolf with Zamanian because the two reference teach away from one another ...".

In response, it is noted and found unconvincing, since both Zamanian and Wolf clearly teach to over-etch of the underlying conductive layer during formation of the contact hole. Although not significant overetching, Wolf clearly teaches the necessity to over-etch the underlying layer. Zamanian also teaches that significant overetch does occur during formation of the contact hole.

Accordingly, although it may not obvious to combine Wolf with Zamanian because the two reference teach away from one another, it still would have been obvious to one of ordinary skill in the art at the time the invention was made to form the contact hole of Okada et al by etching a contact hole in the overlayer insulator and in an overetch amount of the layer of conductive material having a substantially vertical component, as combinatively taught by Zamanian and Toshiyuki, wherein the contact is formed in the overlayer and in said vertical component. This is because of the desirability to insure that all of the dielectric of the overlayer has been completely removed from the contact hole for providing a secure and good electrical connection from the layer of conductive material to the contact. This is also because of the desirability to improve reliability in the multilayer interconnection structure.

*** Regarding Okada in view of Zamanian and Toshiyuki:

Applicant's main remark (at 10/24/02 remark page 5, from last paragraphs) that "...Toshiyuki et al teaches away from forming a vertical component...by stating that the 1st wiring layer 2 is placed on a base that is almost flat...the landing pad having a flat base over the substrate...".

It is noted and found unconvincing. First, it still would have been obvious, since the reference of Zamanian still teaches to overetch the underlying wiring layer during formation of the contact hole. Second, applicant apparently remarks that Toshiyuki teaches to overetch the underlying wiring layer during formation of the contact hole, but the base that is almost flat. In response, Claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. In Re Self, 213 USPQ 1,5 (CCPA 1982); In Re Priest, 199 USPQ 11,15 (CCPA 1978). Nowhere in the claim require any structure for the vertical component. As shown in Figure 5 of the present application, what is a structure of the vertical component as claimed?.

****

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

*** Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (703) 308-2554. The examiner can normally be reached on M-F: 8:30 Am to 5:00 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (703) 308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs

Michael Trinh
Primary Examiner